FACSIMILE

SMC
STANDARD
MICROSYSTEMS
CORPORATION

TO: Aubrey Kagan DATE: 5/11/95

COMPANY: _____ CC: _____

FROM: Mike McEntee _____

_____

FAX NO: _____ _____

SUBJECT: _____

NUMBER OF PAGES TRANSMITTED INCLUDING THIS COVER PAGE: 2. IF YOU HAVE ANY PROBLEMS RECEIVING THIS FAX, PLEASE FAX (516) 273-3123 OR CALL (516) 435-6961 (EXTENSION NUMBER). THANK YOU.

Component Products Division
300 Kennedy Drive
Hauppauge, NY 11788
(516) 273-3100
FAX (516) 231-6004

STANDARD MICROSYSTEMS CORPORATION

[redacted]

July 3, 1991

20020 REV B modifications list

New features:

1) PULSE1* programmable to push pull output in backplane mode.

PULSE1* is an Open Drain output in backplane mode intended to directly drive a backplane. use external drivers and would benefit from a push pull option.
A bit in the setup register will enable it. It defaults to open drain for compatibility purposes.

2) Programmable polarity for TXENABLE.

For RS485 drivers, an active high TXENABLE saves an external inverter.

If the PULSE2* pin is externally grounded, the 20020 will adopt the new active high TXENABLE mode. If PULSE2* is left open, TXENABLE stays as the present active low signal.

3) NEXT ID readable.

The tentative ID based scheme for building a network map would not indicate the next ID as being active. The simplest way around that limitation is to make the Next ID readable. Next ID is the node to which the device will pass the token.
The next ID can be read from offset 7 when the sub address bits in the configuration register are set to 3. It is a read only register.

4) Definition of ET3 allows shorter topologies values for the timers.
When the new bit ET3 is set, timers are 3 times faster, which would support networks delays of about 10usec end to end. Reconfigurations will take 1/3 of the present time.

5) EXC NAK can be programmed to be set after 4 events, as well as the present 128.
6) ADDitionAL clock prescAler AllowS 156.25K BPS

Correction of the following rev A anomalies:

1) TXEN. Rev B will blocking the transmit enable for as long as the TXEN bit is cleared.

2) Pointer readback in read mode. Rev A can give address prefetched rather than address read, after initial read.

3) Eliminate time uncertainty in RCV ACT and TOKEN SEEN bits. (In rev A they can take up to 82 usec to be set).